(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 613 091 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
04.07.2001 Bulletin 2001/27

(51) Int Cl.7: **G06F 13/40**

(21) Application number: **94301362.3**

(22) Date of filing: **25.02.1994**

(54) **Parallel data transfer circuit**

Paralleldatenübertragungsschaltung

Circuit de transmission de données parallèles

(84) Designated Contracting States:
DE FR GB IT NL SE

(30) Priority: **26.02.1993 JP 3853093**

(43) Date of publication of application:
31.08.1994 Bulletin 1994/35

(73) Proprietor: **NEC CORPORATION**
Tokyo (JP)

(72) Inventor: **Kawashima, Takaaki,**
c/o NEC Corporation
Tokyo 108-01 (JP)

(74) Representative: **Abnett, Richard Charles**
REDDIE & GROSE
16 Theobalds Road
London WC1X 8PL (GB)

(56) References cited:
GB-A- 2 119 977 **US-A- 5 057 998**

- **PATENT ABSTRACTS OF JAPAN vol. 013, no. 347 (P-910), 4 August 1989 & JP-A-01 106158 (HITACHI LTD), 24 April 1989,**
- **PATENT ABSTRACTS OF JAPAN vol. 015, no. 349 (P-1247), 4 September 1991 & JP-A-03 132857 (HITACHI SEIKO LTD), 6 June 1991,**

EP 0 613 091 B1

Printed by Jouve, 75001 PARIS (FR)

Description

1. Field of the Invention

[0001] This invention relates to a parallel data transfer circuit which transfers parallel data from a transfer source circuit to a transfer destination circuit in a digital communication apparatus or a like apparatus.

2. Description of the Related Art

[0002] Various parallel data transfer circuits are conventionally known, and an exemplary one of conventional parallel data transfer circuits is shown in FIG. 2. Referring to FIG. 2, in the parallel data transfer circuit shown, parallel data are transferred from a data transfer source circuit 201 to a data transfer destination circuit 202. In order to allow the data transfer source circuit 201 to perform data storage address control of the data transfer destination circuit 202, an address signal 211, an upper byte write signal 212 and a lower byte write signal 213 are sent from the data transfer source circuit 201 to the data transfer destination circuit 202 before parallel data are transferred from the data transfer source circuit 201 to the data transfer destination circuit 202. For transfer of parallel data which include word data of 16 bits and byte data of 8 bits in a mixed condition, it is necessary to prepare a data bus of a word width and provide a change-over circuit such as an upper byte data selector 209 and a lower byte data selector 204 between the data transfer source circuit 201 and the data transfer destination circuit 202 so that an upper byte and a lower byte of the parallel data may be selected. Such changing over is controlled by the data transfer source circuit 201 (refer to, for example, Japanese Patent Laid-Open Application No. Showa 62-32748, No. Showa 62-49735 or No. Heisei 1-238338).

[0003] The parallel data transfer circuit further includes a data bus 214 for 8 bits between the data transfer source circuit 201 and the upper byte data selector 203, another data bus 215 between the data transfer source circuit 201 and the lower byte data selector 204, an upper byte data select signal line 216, a lower byte data select signal line 217, a further data bus 218 for 8 bits between the upper byte data selector 203 and the data transfer destination circuit 202, and a still further data bus 219 between the lower byte data selector 204 and the data transfer destination circuit 202.

[0004] The conventional parallel data transfer circuit described above is disadvantageous in that processing at the data transfer source circuit 201 is complicated and much time is required for transfer since the data transfer source circuit 201 performs changing over between the upper byte data selector 203 and the lower byte data selector 204 and controls the data storage address of the data transfer destination circuit 202 to transfer data.

[0005] Further, the conventional parallel data transfer circuit is also disadvantageous in that, when data are transferred without involving such changing over between data buses, a discontinuous empty portion is produced in the data storage area of the data transfer destination circuit 2 and consequently the data storage area cannot be used effectively.

[0006] United States Patent US-A-5,057,998 describes a data transfer control unit for data transfer between two systems, which uses a dual-port random-access memory. Writing into the memory is indicated by a one-bit access flag. Data is read out in dependence upon the presence or absence of a flag.

[0007] According to the present invention, there is provided a parallel data transfer circuit, which comprises a data transfer source circuit for outputting a register designation signal together with parallel data in a mixed condition of word data of 16 bits and byte data of 8 bits, a plurality of data registers including a plurality of sets of data registers each including a data register for an upper byte and a data register for a lower byte, a plurality of flag registers individually corresponding to the data registers including a plurality of sets of flag registers each including a flag register for an upper byte and a flag register for a lower byte, a write circuit for writing parallel data outputted from the data transfer source circuit into one of the data registers designated by the register designation signal from the data transfer source circuit and placing a flag into one of the flag registers corresponding to the data register, a read circuit for reading data in the data registers and a flag in the flag registers, and a data transfer destination circuit for outputting, after an end signal is received from the data transfer source circuit, a select signal to select one of the data registers and one of the flag registers to read out data in the data register and a flag in the flag register by way of the read circuit, and for fetching the data read out by the read circuit when a flag is held by the flag register corresponding to the data register selected in response to the select signal but refraining from fetching the data when a flag is not held by the flag register.

[0008] In a preferred form of the present invention, the write circuit includes a decoder for decoding the register designation signal from the data transfer source circuit, and a plurality of OR circuits provided for the plurality of data registers and the plurality of flag registers for receiving a signal decoded by the decoder and the write signal outputted from the data transfer source circuit to put a corresponding one of the data registers into a writing condition and place a flag into a corresponding one of the flag registers, and the read circuit includes a data selector for selecting one of the data registers in response to the select signal from the data transfer destination circuit and a flag selector for selecting one of the flag registers in response to the select signal.

[0009] With the parallel data transfer circuit, when data outputted from the data transfer source circuit are written into one of the data registers designated by a register designation signal, a flag is placed into one of the flag registers corresponding to the data register, but

no flag is placed into a register corresponding to one of the data registers into which no data are written. Thus, data only of date registers corresponding to those of the flag registers in which a flag is held are fetched into the data transfer destination circuit, and consequently, the parallel data can be received without forming a discontinuous empty portion in the data storage area of the data transfer destination circuit.

[0010] Further, the data transfer source circuit does not output a signal for controlling the data storage address of the data transfer destination circuit but only outputs, simultaneously with data, a register designation signal for designating those of the data registers and the flag registers which should temporarily latch data between the data transfer source circuit and the data transfer destination circuit, that is, a sequence signal for successively selecting the registers. Consequently, since the data transfer source circuit does not control the data storage address of the data transfer destination circuit at all, processing to be executed by the data transfer source circuit is reduced and the time required for transfer for data is reduced as much.

[0011] The invention will now be described in more detail, by way of example, with reference to the drawings, in which:

FIG. 1 is a block diagram of a parallel data transfer circuit showing a preferred embodiment of the present invention; and

FIG. 2 (described above) is a block diagram showing an outline of a conventional parallel data transfer circuit.

[0012] Referring to FIG. 1, there is shown a parallel data transfer circuit to which the present invention is applied. The parallel data transfer circuit shown includes a data transfer source circuit 1, a data transfer destination circuit 2, a decoder 11, n data register sets DR1 to DRn each composed of a pair of registers 13A and 13B for an upper byte and a lower byte, respectively, n corresponding flag register sets FR1 to FRn each composed of a pair of registers 14A and 14B for an upper byte and a lower byte corresponding to the registers 13A and 13B for an upper byte and a lower byte of each set, respectively, a pair of OR circuits 12A and 12B for an upper byte and a lower byte corresponding to the registers 13A and 14A for an upper byte and the registers 13B and 14B for a lower byte of each set, respectively, a data selector 15, and a flag selector 16.

[0013] In the parallel data transfer circuit, the decoder 11 and the n OR circuits 12A and n OR circuits 12B constitute a write circuit for writing data and a flag, and the data selector 15 and the flag selector 16 constitute a read circuit for reading out data and a flag. Here, the parallel data transfer circuit can transfer three kinds of data including data composed only of an upper byte, data composed only of a lower byte, and word data, and can transfer n words in the maximum in a single transferring operation.

[0014] It is to be noted that, while several signal lines interconnecting the components of the parallel data transfer circuit described above are shown in FIG. 1, each line with a slanting line attached thereto represents that the signal line is actually parallel signal lines for 8 bits.

[0015] When data are to be transferred, the data transfer source circuit 1 outputs a decoder enable signal 101 to put the decoder 11 into an enabled condition and then outputs to the decoder 11 a register designation signal 102 which successively designates required ones of the n data registers and flag registers. Further, when upper byte data 104 and/or lower byte data 105 are to be outputted, the data transfer source circuit 1 simultaneously outputs an upper byte write instruction signal 106 and/or a lower byte write instruction signal 107. Then, after outputting of data for a single transferring cycle (a set of data) is completed, the data transfer circuit 1 outputs a transmission end signal 108 to the data transfer destination circuit 2.

[0016] The decoder 11 decodes the register designation signal 102 from the data transfer source circuit 1 and inputs a write permission signal 103 to the OR circuits 12A and 12B for an upper byte and a lower byte of the set designated by the register designation signal 102. In the set to which the write permission signal 103 is inputted, if an upper byte write instruction signal 106 is outputted simultaneously from the data transfer source circuit 1, a write signal 116 is outputted from the OR circuit 12A for an upper byte to write upper byte data 104 from the data transfer source circuit 1 into the data register 13A for an upper byte and place a flag into the flag register 14A for an upper byte. On the other hand, if a lower byte write instruction signal 107 is outputted simultaneously from the data transfer source circuit 1, a write signal 117 is outputted from the OR circuit 12B for a lower byte to write lower byte data 105 from the data transfer source circuit 1 into the data register 13B for a lower byte and place a flag into the flag register 14B for a lower byte.

[0017] When a transmission end signal 108 is received from the data transfer source circuit 1, the data transfer destination circuit 2 outputs a select signal 111 to the data selector 15 and the flag selector 16. In response to the select signal 111, the data selector successively selects the n data register sets DR1 to DRn for each of the registers 13A and 13B to read out data and outputs the data as read data 112 to the data transfer destination circuit 2. Meanwhile, the flag selector 16 successively selects, in response to the select signal 111, the n flag register sets FR1 to FRn for each of the registers 14A and 14B to read out a flag and outputs the flag as a flag read signal 113 to the data transfer destination circuit 2.

[0018] The data transfer destination circuit 2 fetches the read data 112 from the data selector 15, that is, data read out from the data register selected in response to

the select signal 111, when the flag read signal 113 from the flag selector 16 is "flag present" representing presence of a flag, that is, when a flag is held in the flag register selected in response to the select signal 111. On the contrary when the flag read signal 113 is "flag absent" representing absence of a flag, that is, when no flag is held in the flag register selected in response to the select signal 111, the data transfer destination circuit 2 refrains from fetching the data from the data register selected in response to the select signal 111. In other words, the data transfer destination circuit 2 fetches data only from the register 13A or 13B corresponding to the register 14A or 14B in which a flag is held. Accordingly, no discontinuous empty portion is produced in the data storage area of the data transfer destination circuit 2.

[0019] After the data fetching operation from all of the register sets DR1 to DRn is completed, the data transfer source circuit 2 outputs a reception end signal 115 to the data transfer source circuit 1 and outputs a reset signal 114 to the registers 14A and 14B of all of the flag register sets FR1 to FRn.

[0020] Subsequently, an operation for writing only upper byte data, another operation for writing only lower byte data and a further operation for writing word data into a data register will be described.

<Writing Only of Upper Byte Data>

[0021]

1. A decoder enable signal 101 is outputted from the data transfer source circuit 1 to put the decoder 11 into an enabled condition.
2. A register designation signal 102 which designates, for example, a first register set is outputted from the decoder transfer source circuit 1 to the decoder 11.
3. A write permission signal 103 for the first set is outputted from the decoder 11, and an upper byte write instruction signal 106 is outputted from the data transfer source circuit 1.
4. A write signal 116 is outputted from the OR circuit 12A for an upper byte of the first set to put the register 13A for an upper byte of the first register set DR1 and the register 14A for an upper byte of the first flag register set FR1 into a write enabled condition.
5. Upper byte data 104 are outputted from the data transfer source circuit 1 and latched by the register 13A for an upper byte of the first data register set DR1, and a flag is placed into the register 14A for an upper byte of the first flag register set FR1.

<Writing Only of Lower Byte Data>

[0022]

1. A decoder enable signal 101 is outputted from the data transfer source circuit 1 to put the decoder 11 into an enabled condition.
2. A register designation signal 102 which designates, for example, a second register set is outputted from the decoder transfer source circuit 1 to the decoder 11.
3. A write permission signal 103 for the second set is outputted from the decoder 11, and an upper byte write instruction signal 106 is outputted from the data transfer source circuit 1.
4. A write signal 117 is outputted from the OR circuit 12B for a lower byte of the second set to put the register 13B for a lower byte of the second register set DR2 and the register 14B for a lower byte of the second flag register set FR2 into a write enabled condition.
5. Lower byte data 105 are outputted from the data transfer source circuit 1 and latched by the register 13B for a lower byte of the second data register set DR2, and a flag is placed into the register 14B for a lower byte of the second flag register set FR2.

<Writing of Word Data>

[0023]

1. A decoder enable signal 101 is outputted from the data transfer source circuit 1 to put the decoder 11 into an enabled condition.
2. A register designation signal 102 which designates, for example, a third register set is outputted from the decoder transfer source circuit 1 to the decoder 11.
3. A write permission signal 103 for the third set is outputted from the decoder 11, and an upper byte write instruction signal 106 and a lower byte write instruction signal 107 are outputted from the data transfer source circuit 1.
4. Write signals 116 and 117 are outputted from the OR circuit 12A for an upper byte and the OR circuit 12B for a lower byte of the third set to put the register 13A for an upper byte and the register 13B for a lower byte of the third register set DR3 and the register 14A for an upper byte and the register 14B for a lower byte of the third flag register set FR3 into a write enabled condition, respectively.
5. Upper byte data 104 are outputted from the data transfer source circuit 1 and latched by the register 13A for an upper byte of the third data register set DR3 and lower byte data 105 are latched by the register 13B for a lower byte of the third data register set DR3, and a flag is placed into each of the the register 14A for an upper byte and the register 14B

for a lower byte of the third flag register set FR3.

[0024] Subsequently, a reading operation for the data registers will be described by way of an example wherein only upper byte data are latched in the first data register set DR1 and only lower byte data are latched in the second data register set DR2 while word data are latched in the third data register set DR3 as a result of the writing operation described above.

1. The data transfer destination circuit 2 first outputs, to the data selector 15 and the flag selector 16, a select signal 111 to select the register 13A for an upper byte of the first data register set DR1 and the register 14A for an upper byte of the first flag register set FR1.
2. The data selector 15 reads out data of the register 13A for an upper byte of the first data register set DR1 and outputs the read data 112 while the flag selector 16 reads out a flag of the register 14A for an upper byte of the first flag register set FR1 and outputs a flag read signal 113 of "flag present".
3. The data transfer destination circuit 2 fetches the read data 112 from the data selector 15 since the flag read signal 113 is "flag present".
4. Then, the data transfer destination circuit 2 outputs a select signal 111 to select the register 13B for a lower byte of the first data register set DR1 and the register 14B for a lower byte of the first flag register set FR1.
5. The data register 15 reads out data of the register 14B for a lower byte of the first data register set DR1 and outputs the read data 112 while the flag selector 16 reads out a flag of the register 14B for a lower byte of the first flag register set FR1 and outputs a flag read signal 113 of "flag absent".
6. The data transfer destination circuit 2 refrains from fetching the read data 112 since the flag read signal 113 is "flag absent".
7. Subsequently, the data transfer destination circuit 2 outputs a select signal 111 to select the register 13A for an upper byte of the second data register set DR2 and the register 14A for an upper byte of the second flag register set FR2.
8. The data selector 15 reads out data of the register 13A for an upper byte of the second data register set DR2 and outputs the read data 112 while the flag selector 16 reads out a flag of the register 14A for an upper byte of the second flag register set FR2 and outputs a flag read signal 113 of "flag absent".
9. The data transfer destination circuit 2 refrains from fetching the read data 112 since the flag read signal 113 is "flag absent".
10. Then, the data transfer destination circuit 2 outputs a select signal 111 to select the register 13B for a lower byte of the second data register set DR2 and the register 14B for a lower byte of the second flag register set FR2.
11. The data selector 15 reads out data of the register 13B for a lower byte of the second data register set DR2 and outputs the read data 112 while the flag selector 16 reads out a flag of the register 14B for a lower byte of the second flag register set FR2 and outputs a flag read signal 113 of "flag present".
12. The data transfer destination circuit 2 fetches the read data 112 since the flag read signal 113 is "flag present".
13. Then, the data transfer destination circuit 2 outputs a select signal 111 to select the register 13A for an upper byte of the third data register set DR3 and the register 14A for an upper byte of the third flag register set FR3.
14. The data selector 15 reads out data of the register 13A for an upper byte of the third data register set DR3 and outputs the read data 112 while the flag selector 16 reads out a flag of the register 14A for an upper byte of the third flag register set FR3 and outputs a flag read signal 113 of "flag absent".
15. The data transfer destination circuit 2 refrains from fetching the read data 112 since the flag read signal 113 is "flag absent".
16. Subsequently, the data transfer destination circuit 2 outputs a select signal 111 to select the register 13B for a lower byte of the third data register set DR3 and the register 14B for a lower byte of the third flag register set FR3.
17. The data selector 15 reads out data of the register 13B for a lower byte of the third data register set DR3 and outputs the read data 112 while the flag selector 16 reads out a flag of the register 14B for a lower byte of the third flag register set FR3 and outputs a flag read signal 113 of "flag present".
18. The data transfer destination circuit 2 fetches the read data 112 since the flag read signal 113 is "flag present".

[0025] The parallel data transfer circuit illustrated has the advantage that processing at the data transfer source circuit is simplified, thus reducing the time required for transfer. Also, the formation of discontinuous empty portions in the data storage area of the data transfer destination circuit is avoided, allowing more effective use of the data storage area.

[0026] Having now fully described the invention, it will be apparent to one of ordinary skill in the art that many changes and modifications can be made thereto without departing from the scope of the invention as set forth herein.

Claims

1. A parallel data transfer circuit, comprising:

a data transfer source circuit (1) for outputting a register designation signal together with par-

allel data in a mixed condition of word data of 16 bits and byte data of 8 bits;
a plurality of data registers (13A, 13B) including a plurality of sets (DR1 to DRn) of data registers each including a data register for an upper byte and a data register for a lower byte;
a plurality of flag registers (14A, 14B) individually corresponding to said data registers (13A, 13B) including a plurality of sets (FR1 to FRn) of flag registers each including a flag register for an upper byte and a flag register for a lower byte;
a write circuit (11, 12A, 12B) for writing parallel data outputted from said data transfer source circuit (1) into one of said data registers (13A, 13B) designated by the register designation signal from said data transfer source circuit (1) and placing a flag into one of said flag registers (14A, 14B) corresponding to the data register;
a read circuit (15, 16) for reading data in said data registers (13A, 13B) and a flag in said flag registers (14A, 14b); and
a data transfer destination circuit (2) for outputting, after an end signal is received from said data transfer source circuit (1), a select signal to select one of said data registers (13A, 13B) and one of said flag registers (14A, 14B) to read out data in the data register and a flag in the flag register by way of said read circuit (15, 16), and for fetching the data read out by said read circuit (15, 16) when a flag is held by the flag register corresponding to the data register selected in response to the select signal but refraining from fetching the data when a flag is not held by the flag register.

2. A parallel data transfer circuit as set forth in claim 1, in which said write circuit (11, 12A, 12B) includes a decoder (11) for decoding the register designation signal from said data transfer source circuit (1), and a plurality of OR circuits (12A, 12B) provided for said plurality of data registers (13A, 13B) and said plurality of flag registers (14A, 14B) for receiving a signal decoded by said decoder and the write signal outputted from said data transfer source circuit (1) to put a corresponding one of said data registers (13A, 13B) into a writing condition and place a flag into a corresponding one of said flag registers (14A, 14B), and said read circuit (15, 16) includes a data selector (15) for selecting one of said data registers (13A, 13B) in response to the select signal from said data transfer destination circuit (2) and a flag selector (16) for selecting one of said flag registers (14A, 14B) in response to the select signal.

Revendications

1. Circuit de transmission de données parallèles, comprenant :

   - un circuit source de transmission de données (1) pour sortir un signal de désignation de registre conjointement avec des données parallèles dans un état mixte de données de mot de 16 bits et de données d'octet de 8 bits ;
   - une pluralité de registres de données (13A, 13B) incluant une pluralité de jeux (DR1 à DRn) de registres de données, chacun incluant un registre de données pour un octet supérieur et un registre de données pour un octet inférieur ;
   - une pluralité de registres de drapeau (14A, 14B) correspondant individuellement auxdits registres de données (13A, 13B), incluant une pluralité de jeux (FR1 à FRn) de registres de drapeau, chacun incluant un registre de drapeau pour un octet supérieur et un registre de drapeau pour un octet inférieur ;
   - un circuit d'écriture (11, 12A, 12B) pour écrire des données parallèles sorties dudit circuit source de transmission de données (1) dans un desdits registres de données (13A, 13B) désigné par le signal de désignation de registre provenant dudit circuit source de transmission de données (1) et placer un drapeau dans un desdits registres de drapeau (14A, 14B) correspondant au registre de données ;
   - un circuit de lecture (15, 16) pour lire des données dans lesdits registres de données (13A, 13B) et un drapeau dans lesdits registres de drapeau (14A, 14B) ; et
   - un circuit de destination de transmission de données (2) pour sortir, après qu'un signal de fin a été reçu depuis ledit circuit source de transmission de données (1), un signal de sélection afin de sélectionner un desdits registres de données (13A, 13B) et un desdits registres de drapeau (14A, 14B) afin de lire des données dans le registre de données et un drapeau dans le registre de drapeau au moyen dudit circuit de lecture (15, 16), et pour prélever les données lues par ledit circuit de lecture (15, 16) lorsqu'un drapeau est maintenu par le registre de drapeau correspondant au registre de données sélectionné en réponse au signal de sélection mais s'abstenir de prélever les données lorsqu'un drapeau n'est pas maintenu par le registre de drapeau.

2. Circuit de transmission de données parallèles selon la revendication 1, dans lequel :

   - ledit circuit d'écriture (11, 12A, 12B) inclut un décodeur (11) pour décoder le signal de dési-

gnation de registre provenant dudit circuit source de transmission de données (1) et une pluralité de circuits OU (12A, 12B) prévus pour ledite pluralité de registres de données (13A, 13B) et ladite pluralité de registres de drapeau (14A, 14B) pour recevoir un signal décodé par ledit décodeur et le signal d'écriture sorti dudit circuit source de transmission de données (1) afin de positionner un registre correspondant desdits registres de données (13A, 13B) dans un état d'écriture et de placer un drapeau dans un registre correspondant desdits registres de drapeau (14A, 14B) ; et

ledit circuit de lecture (15, 16) inclut un sélecteur de données (15) pour sélectionner un desdits registres de données (13A, 13B) en réponse au signal de sélection provenant dudit circuit de destination de transmission de données (2) et un sélecteur de drapeau (16) pour sélectionner un desdits registres de drapeau (14A, 14B) en réponse au signal de sélection.

Patentansprüche

1. Paralleldatenübertragungsschaltung mit:

einer Datenübertragungsausgangsschaltung (1) zum Ausgeben eines Registerbezeichnungssignals zusammen mit Paralleldaten in einem Mischzustand von Wortdaten mit 16 Bits und Bytedaten mit 8 Bits;
mehreren Datenregistern (13A, 13B) mit mehreren Sätzen (DR1 bis DRn) von Datenregistern, die jeweils ein Datenregister für ein oberes Byte und ein Datenregister für ein unteres Byte aufweisen;
mehreren Flagregistern (14A, 14B), die einzeln den Datenregistern (13A, 13B) entsprechen, mit mehreren Sätzen (FR1 bis FRn) von Flagregistern, die jeweils ein Flagregister für ein oberes Byte und ein Flagregister für ein unteres Byte aufweisen;
einer Schreibschaltung (11, 12A, 12B) zum Schreiben von Paralleldaten, die von der Datenübertragungsausgangsschaltung (1) ausgegeben werden, in eines der Datenregister (13A, 13B), das durch das Registerbezeichnungssignal von der Datenübertragungsausgangsschaltung (1) bezeichnet ist, und Setzen eines Flags in einem der Flagregister (14A, 14B), das dem Datenregister entspricht;
einer Leseschaltung (15, 16) zum Lesen von Daten in den Datenregistern (13A, 13B) und eines Flags in den Flagregistern (14A, 14B); und
einer Datenübertragungszielschaltung (2) zum nach Empfang eines Endesignals von der Datenübertragungsausgangsschaltung (1) erfolgenden Ausgeben eines Auswahlsignals, um eines der Datenregister (13A, 13B) und eines der Flagregister (14A, 14B) auszuwählen, um Daten im Datenregister und ein Flag im Flagregister über die Leseschaltung (15, 16) auszulesen, und zum Abrufen der durch die Leseschaltung (15, 16) ausgelesenen Daten, wenn ein Flag durch das Flagregister gehalten wird, das dem als Reaktion auf das Auswahlsignal ausgewählten Datenregister entspricht, aber zum Nichtabrufen der Daten, wenn ein Flag nicht durch das Flagregister gehalten wird.

2. Paralleldatenübertragungsschaltung nach Anspruch 1, wobei die Schreibschaltung (11, 12A, 12B) aufweist: einen Decodierer (11) zum Decodieren des Registerbezeichnungssignals von der Datenübertragungsausgangsschaltung (1) und mehrere ODER-Schaltungen (12A, 12B), die für die mehreren Datenregister (13A, 13B) und die mehreren Flagregister (14A, 14B) vorgesehen sind, zum Empfangen eines durch den Decodierer decodierten Signals und des von der Datenübertragungsausgangsschaltung (1) ausgegebenen Schreibsignals, um ein entsprechendes der Datenregister (13A, 13B) in einen Schreibzustand zu versetzen und ein Flag in einem entsprechenden der Flagregister (14A, 14B) zu setzen, und die Leseschaltung (15, 16) aufweist: einen Datenselektor (15) zum Auswählen eines der Datenregister (13A, 13B) als Reaktion auf das Auswahlsignal von der Datenübertragungszielschaltung (2) und einen Flagselektor (16) zum Auswählen eines der Flagregister (14A, 14B) als Reaktion auf das Auswahlsignal.

FIG.1

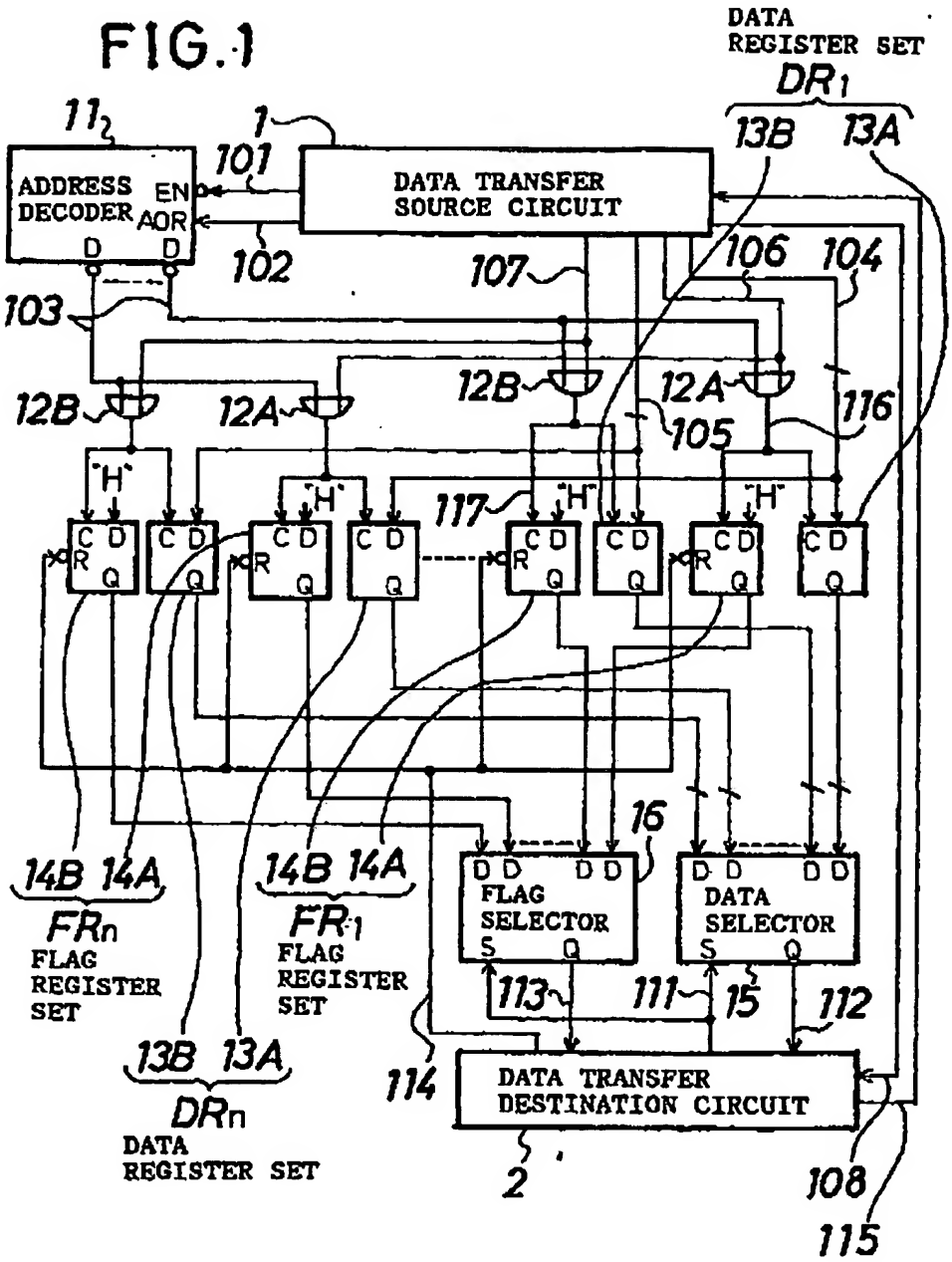
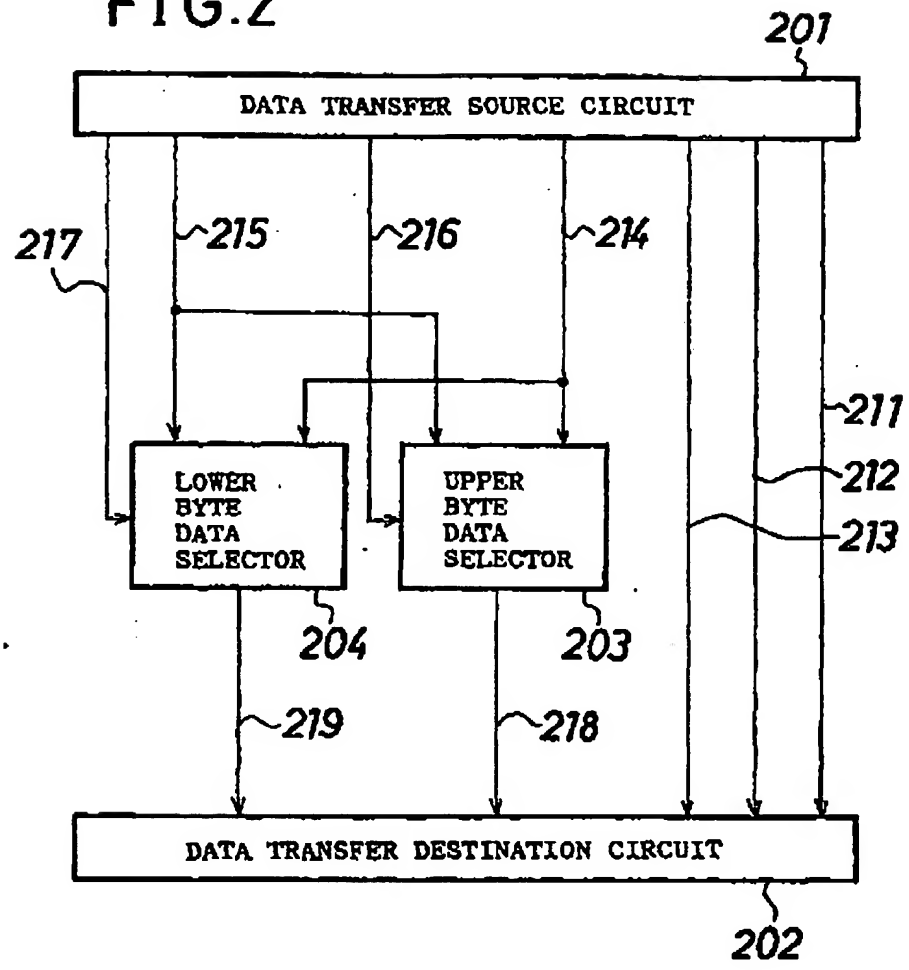


FIG.2



HP040112PDE April 7, 2005

TRANSLATION INTO ENGLISH OF:

OFFICE ACTION

Of : March 8, 2005
Applicant : Hewlett-Packard Development Co., L.P.
Application No. : 10 2004 003 867.8-53

The number of the following reference is cited in this Office Action for the first time and will be used throughout the examination proceedings:

1) EP 0 613 091 B1

I.

Reference (1) (cf. Fig. 2 and the associated description) discloses a data selection circuit which is connected to a data bus (214, 215) and which comprises a "logic" (selector 203, 204) for receiving data consisting of a plurality of block-aligned N-bit portions (lower and upper bytes) and for outputting a designated one of the N-bit portions (either lower-byte or upper-byte data via 219, 218), and a circuitry for providing to the receiving logic a control signal (216, 217) for designating one of the N-bit portions (supplied from the DATA TRANSFER SOURCE CIRCUIT 201). That the data specified in claim 1 are debug data and that the data selection circuit is used for a "general purpose performance counter" cannot substantiate an inventive step for the subject matter of claim 1, in particular in view of the fact that it is unclear what a "general purpose performance counter" ("Mehrzweck-Leistungszähler") is, (What is the "general purpose" ("Mehrzweck") ? Is the "counter" supposed to fulfil also functions other than the counting function, or is it supposed to count also magnitudes other than the "performance" ("Leistung")? Which "performance" ("Leistung") is meant? The power consumption perhaps?), and in particular also in view of the fact that the data selection circuit known from reference 1, i.e. a conventional selector or multiplexer, can be used independently of the type of data and the intended use.
Claim 1 is therefore not allowable.
Claims 2 to 8, which depend on claim 1, must be rejected together with said claim 1.
The features of claims 2 and 3 are also known from reference 1 (a multiplexer is nothing else but a selector).

Claim 9 is formulated as a parallel claim. Parallel claims are, however, only admissible if they contain a solution of the same task which is independent of the solution of the main claim. This condition is not fulfilled in the present case, since claim 9 differs from claim 1 only insofar as the designations "logic" (what is to be understood by this designation?) and circuitry have been replaced by the common term "means", said means executing the same functions as the "special" means referred to in claim 1.
It follows that claim 9 is not allowable – not least for formal reasons.
Claims 10 to 16, which depend on said claim 9, must be rejected together therewith.

Claim 17 concerns a method of implementing data selection and the method steps claimed only describe the functions of the data selection circuit which have already been specified in claim 1. It follows that the factual content of claim 17 does not exceed that of claim 1. This means that reference 1 has to be considered as relevant prior art also with regard to said claim 17. Hence, also the method according to claim 17 fails to be based on an inventive step.
Claim 17 is therefore not allowable.
Claims 18 to 22, which depend on said claim 17, must be rejected together therewith.

II.

If the applicant should be of the opinion that the application still contains features having an importance that could substantiate the grant of a patent, he is requested to substantiate this in detail and to submit a new main claim which is directed to these features as well as sub-claims which are adapted to said main claim.

III.

If the set of claims is maintained or if a set of claims is submitted in which the Examiner's objections have not been taken into account to a sufficient extent, rejection of the application will have to be reckoned with.

Encl.
copy of 1 reference

Patent Examiner for class G 06 F
Dipl.-Ing. Hafner